## CLAIMS

What is claimed is:

1. A method for generating a wafer level burn-in reliability curve, comprising:

detecting a signal indicating a transition associated with one of a number *m* of cycles of burn-in testing of a wafer;

storing a time stamp associated with said transition in nonvolatile memory in each integrated circuit (IC) die on said wafer;

performing a built-in self test (BIST) to determine a current number of failures in each said IC die associated with said time stamp;

storing said current number of failures in each said IC die associated with said time stamp in said nonvolatile memory in each said IC die;

repeating the foregoing for at least one additional cycle of burn-in testing; and

reading said time stamp and current number of failures associated with said time stamp for each of said time stamps.

2. The method according to claim 1, wherein said signal indicating a transition associated with one of said number *m* of cycles of burn-in testing comprises a supervoltage signal.

3. The method according to claim 1, wherein said number m of cycles comprises four quarters of burn-in testing.

4. The method according to claim 1, wherein said transition occurs before a first time stamp, between two consecutive time stamps or after a last time stamp of said number *m* of cycles of burn-in testing.

5. The method according to claim 1, wherein said wafer comprises a plurality of integrated circuits.

6. The method according to claim 5, wherein each of said plurality of integrated circuits comprises a memory device.

7. The method according to claim 1, wherein said reading said time stamp and current number of failures associated with said time stamp for each of said time stamps comprises reading nonvolatile elements at wafer probe testing.

8. The method according to claim 1, further comprising generating said wafer burn-in reliability curve from said time stamp and said current number of failures associated with said time stamp for each of said time stamps.

9. A method for testing a wafer having integrated circuit (IC) dice formed thereon, comprising:

stressing said IC dice;

storing wafer level burn-in reliability data in nonvolatile elements in each IC die on said wafer; and

performing a wafer probe procedure comprising:

executing a functional test to identify error-free IC dice and repairable IC dice from said IC dice;

repairing all repairable IC dice; and

reading wafer level burn-in reliability data stored in said nonvolatile elements.

10. The method according to claim 9, wherein said stressing, storing and performing are performed in the order stated.

11. The method according to claim 9, wherein said stressing comprises using built-in self-stress circuitry in each IC die.

12. The method according to claim 9, further comprising generating burn-in reliability curves from said wafer level burn-in reliability data.

13. The method according to claim 12, further comprising determining whether to scrap said wafer, to scrap a lot including said wafer or identify a need for additional burn-in.

14. The method according to claim 9, wherein said stressing said IC dice comprises elevating a power supply voltage with respect to a nominal operating voltage.

15. The method according to claim 9, further comprising:

forming a sacrificial metal layer for delivering power to said IC dice on said wafer prior to stressing; and

removing said sacrificial metal layer from said wafer prior to performing said wafer probe procedure.

16. A memory device comprising:

a memory array;

address compression circuitry in communication with said memory array for compressing memory array addresses into redundancy space;

nonvolatile elements for storing wafer level burn-in data; and

burn-in control circuitry in communication with said memory array, said address compression circuitry and said nonvolatile elements for controlling wafer level burn-in and storing wafer level burn-in data in said nonvolatile elements.

17. The memory device according to claim 16, further comprising signal detection circuitry in communication with said burn-in control circuitry for detecting a signal indicating a transition between wafer level burn-in self-stress and self-test modes.

18. The memory device according to claim 17, further comprising built-in self-stress (BISS) and built-in self-test (BIST) circuitry in communication with said nonvolatile elements, said address compression circuitry, said burn-in control circuitry and said memory array for controlling said wafer level burn-in self-stress and self-test modes.

19. The memory device according to claim 16, wherein said nonvolatile elements comprise antifuse registers.

20. The memory device according to claim 16, wherein said antifuse registers comprise a number $m + 1$ of $n$-bit antifuse registers for storing failures detected before and after $m$ cycles of wafer level burn-in, wherein $m$ and $n$ each comprise positive integers.

21. The memory device according to claim 20, wherein each of said $n$-bit antifuse registers comprises one bit for a time stamp and $n - 1$ bits for storing a binary number of failures detected.

22. The memory device according to claim 16, wherein said redundancy space comprises row redundancy space or column redundancy space.

23. The memory device according to claim 16, wherein a wafer level burn-in reliability curve may be generated from said wafer level burn-in data.

24. A method for storing numbers of failures detected in an integrated circuit (IC) die on a bulk substrate at discrete time intervals during wafer level burn-in, comprising:
providing nonvolatile elements for storing wafer level burn-in data in said IC die;
providing built-in self-stress (BISS) circuitry in said IC die;
providing built-in self-test (BIST) circuitry in said IC die;
initially testing said IC die using said BIST circuitry;
storing a number of failures detected in said nonvolatile elements;
stressing said IC die using said BISS circuitry;
testing said IC die using said BIST circuitry; and
repeating as stated above until a predetermined number of cycles of wafer level burn-in are completed.

25. A method for switching between built-in self-stress (BISS) mode and built-in self-test (BIST) mode in an integrated circuit (IC) during wafer level burn-in, comprising detecting a supervoltage on a nonvolatile programming supply.

26. A method of screening unused antifuse registers during wafer level burn-in, comprising reading a time stamp bit for each antifuse register to determine whether each said antifuse register has been used or has not been used.